CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

1. A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal, in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:

a master clock producing a master clock signal having a frequency greater than the frequency of the DCE clocking signal;

a clock generator deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

a sample enable generator for generating a first sample enable signal at a first time and a second sample enable signal at a second time; and

a sample comparator for using said first sample enable signal and said second enable signal to obtain a first sample of said DTE data signal at said first time and a second sample of said DTE data signal at said second time, and for determining whether the DTE data signal has undergone a transition during the time interval between said first time and said second time.

2. The circuit of claim 1, wherein the frequency of said master clocking signal is approximately 8 times the frequency of said DCE clocking signal.

3. The circuit of claim 1, wherein the time interval between said first time and said second time is approximately 1/8 of the period of said DCE clocking signal.

4. The circuit of claim 1, wherein said sample comparator generates a selector control signal if said first sample is different from said second sample.

5. The circuit of claim 4, further comprising:

an inverter producing an inverted circuit clocking signal from said circuit clocking signal; and

a selector producing an output signal that is selected from the group consisting of said circuit clocking signal and said inverted circuit clocking signal, in response to said selector control signal.

6. A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal, in a communication environment wherein the DCE interfaces the DTE to a communication channel, the circuit comprising:

means for obtaining a first sample of said DTE data signal at a first time;

means for obtaining a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal; and

means for comparing said first sample to said second sample.

7. The circuit of claim 6, wherein the interval between said first time and said second time is approximately 1/8 of the period of the DCE clocking signal.

8. The circuit of claim 6, further comprising:

means for generating a selector control signal if said first sample is different from said second sample.

9. The circuit of claim 8, further comprising:

means for inverting said DCE clocking signal in response to said selector control signal.

10. The circuit of claim 9, further comprising:

means for transmitting said inverted DCE clocking signal from said DCE to said DTE in lieu of said DCE clocking signal.

11. A method for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal, in a communication environment wherein the DCE interfaces the DTE to a communication channel, the method comprising the steps of:

obtaining a first sample of said DTE data signal at a first time;

obtaining a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal; and

comparing said first sample to said second sample.

12. The method of claim 11, wherein the interval between said first time and said second time is approximately 1/8 of the period of the DCE clocking signal.

13. The method of claim 11, further comprising the step of:

generating a selector control signal if said first sample is different from said second sample.

14. The method of claim 13, further comprising the step of:

inverting said DCE clocking signal in response to said selector control signal.

15. The method of claim 14, further comprising the step of:

transmitting said inverted DCE clocking signal from said DCE to said DTE in lieu of said DCE clocking signal.